Listing of Claims

1. (Currently Amended) An apparatus comprising:

a transistor to store data, wherein:

a gate of the transistor is configured to receive a first control signal;

a first channel interface of the transistor is configured to receive a data signal; and

a second channel interface of the transistor is configured to receive a second control signal, the data being stored in the transistor by resetting a floating body of the transistor and then writing the data to the floating body, the floating body being reset when the second control signal assumes a first value, the first value being lower than a second value which the second control signal assumes when the data is written into the floating body, and wherein the first channel interface is a drain and the second channel interface is a source of the transistor.

2. (Original) The apparatus of claim 1, wherein the apparatus is a memory device.

3. (Original) The apparatus of claim 2, wherein the memory device is a dynamic random access memory device.

4. (Original) The apparatus of claim 3, wherein the dynamic random access memory device is a floating body dynamic random access memory device.

5. (Canceled)

6. (Original) The apparatus of claim 1, wherein:

the first channel interface is a drain; and

the second channel interface is a source.

7. (Original) The apparatus of claim 1, wherein:

the first channel interface is a source; and

the second channel interface is a drain.

8. (Original) The apparatus of claim 1, wherein a word line is coupled to the gate of the transistor.

9. (Original) The apparatus of claim 1, wherein a bit line is coupled to the first channel interface of the transistor.

10. (Original) The apparatus of claim 2, wherein a purge line is coupled to the second channel interface of the transistor.

11. (Canceled)

12. (Currently Amended) The apparatus of claim 1, wherein ~~said resetting the floating body of the transistor comprises receiving~~ the first value corresponds to a first voltage level at the second channel interface of the transistor.

13. (Original) The apparatus of claim 12, wherein the first voltage level is part of the second control signal.

14. (Original) The apparatus of claim 12, wherein the first voltage level is in a range of -0.5V to -2.5V.

15. (Original) The apparatus of claim 12, wherein said resetting the floating body of the transistor comprises receiving a second voltage level at the gate of the transistor.

16. (Original) The apparatus of claim 15, wherein the second voltage level is part of the first control signal.

17. (Original) The apparatus of claim 15, wherein the second voltage level is in a range of -.5V to -2.5V.

18. (Original) The apparatus of claim 15, wherein the first voltage level and the second voltage level are received at the transistor overlapping in time.

19. (Previously Presented) The apparatus of claim 1, wherein said writing data to the floating body of the transistor comprises receiving a third voltage level at the first channel interface of the transistor.

20. (Original) The apparatus of claim 19, wherein the third voltage level is part of the data signal.

21. (Original) The apparatus of claim 19, wherein:

the third voltage level is approximately 0V if data written to the transistor represents a logical 0; and

the third voltage level is in a range of 0.5V to 2.5V if data written to the transistor represents a logical 1.

22. (Original) The apparatus of claim 19, wherein said writing data to the floating body of the transistor comprises:

receiving a fourth voltage level at the second channel interface of the transistor; and

receiving a fifth voltage level at the gate of the transistor.

23. (Original) The apparatus of claim 22, wherein:

the fourth voltage level is part of the second control signal; and

the fifth voltage level is part of the first control signal.

24. (Original) The apparatus of claim 22, wherein the third voltage level, the fourth voltage level, and the fifth voltage level are received at the transistor overlapping in time.

25. (Original) The apparatus of claim 22, wherein the fourth voltage level is approximately –0.5V to 0V.

26. (Original) The apparatus of claim 22, wherein the fifth voltage level is in a range of 0.5V to 2.5V.

27. (Currently Amended) A method comprising:

resetting a floating body of the transistor with a first set of control signals overlapping in time; and

selectively writing data to the floating body of the transistor with a second set of control signals and a data signal overlapping in time, the first set of control signals and the second set of control signals being received at a gate of the transistor and a source of the transistor, and the data signal is received at a drain of the transistor,

the first set of control signals including a purge signal coupled to the source of the transistor, the purge signal having a first value lower than a second value which is coupled to the source when the data is selectively written to the floating body of the transistor.

28. (Canceled)

29. (Currently Amended) A system comprising:

a die comprising a processor; and

an off-die component in communication with the processor;

wherein the processor comprises a transistor to store data, wherein:

a gate of the transistor is configured to receive a first control signal;

a first channel interface of the transistor is configured to receive a data signal; and

a second channel interface of the transistor is configured to receive a second control signal, the data being stored in the transistor by resetting a floating body of the transistor and then writing the data to the floating body, the floating body being reset when the second control signal assumes a first value, the first value being lower than a second value which the

second control signal assumes when the data is written into the floating body, and wherein the first channel interface is a drain and the second channel interface is a source of the transistor.

30. (Original) The system of claim 29, wherein the off-die component is at least one of a cache memory, a chip set, and a graphical interface.

31. (New) The apparatus of claim 17, wherein the first and second voltage levels are a same voltage level.

32. (New) A memory cell, comprising:

a transistor including:

(a) a gate coupled to a word line,

(b) a drain coupled to a bit line,

(c) a source coupled to a purge line, and

(d) a floating body between the source and drain,

the purge line assuming a first value during a reset operation and a second value when data is stored in the floating body during a write operation, the first value being lower than the second value.

33. (New) The memory cell of claim 32, wherein the word line assumes the first value and the bit line assumes the second value during the reset operation.

34. (New) The memory cell of claim 32, wherein the first value lies in a negative voltage range.

35. (New) The memory cell of claim 34, wherein the negative voltage range includes -0.5 V. to -2.5V.

36. (New) The memory cell of claim 32, wherein the word line and purge line assume the second value and the bit line assumes the second value or a greater value during a hold operation.

37. (New) The memory cell of claim 32, wherein the bit line assumes the second value and the word line assumes a third value during the reset operation, the first value and the third value both included in a negative voltage range.

38. (New) The memory cell of claim 37, wherein the negative voltage range includes -0.5 V to – 2.5V.

39. (New) The memory cell of claim 38, wherein the first and third values are a same value.